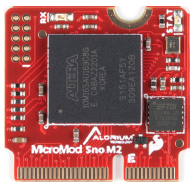

MicroMod Sno M2 Processor Board Pin Map

Last Updated: April 21, 2022

FPGA PINS/SIGNALS			BOARD PINS/SIGNALS				FPGA PINS/SIGNALS		
Sno M2 I/O	Signal	FPGA Pin	Board Function	Board Pin	Board Pin	Board Function	FPGA Pin	Signal	Sno M2 I/O
Not connected to FPGA			3.3V	74	73	G5/BUS5	G4	D1	PORT_D[1]
Not connected to FPGA			RTC_3V_BATT	72	71	G6/BUS6	E13	D2	PORT_D[2]
PORT_H[0]	D42	E12	SPI_CSI/SDIO_DATA3	70	69	G7/BUS7	F13	D3	PORT_D[3]
PORT_H[1]	D43	D12	SDIO_DATA2	68	67	G8	D11	D4	PORT_D[4]
PORT_H[2]	D44	B12	SDIO_DATA1	66	65	G9/ADC_D-/CAM_HSYNC	A12	D5	PORT_D[5]
PORT_H[3]	D45	A11	SPI_SDI1/SDIO_DATA0	64	63	G10/ADC_D+/CAM_VSYNC	A10	D6	PORT_D[6]
PORT_H[4]	D46	A9	SPI_SDO1/SDIO_CMD	62	61	SPI_SDI	A8	D11/MISO	PORT_B[3]
PORT_H[5]	D47	C9	SPI_SCK1/SDIO_CLK	60	59	SPI_SDO	A7	D12/MOSI	PORT_B[4]
PORT_H[6]	D48	A6	AUD_MCLK	58	57	SPI_SCK	A2	D13/SCK	PORT_B[5]
PORT_H[7]	D49	A3	AUD_OUT/CAM_MCLK	56	55	SPI_CS	A4	D10/SCS	PORT_B[2]
PORT_A[0]	D22	B6	AUD_IN/CAM_PCLK	54	53	I2C_SCL1	B2	D9	PORT_B[1]
PORT_A[1]	D23	B3	AUD_LRCLK	52	51	I2C_SDA1	B4	D8	PORT_B[0]
PORT_A[2]	D24	B5	AUD_BCLK	50	49	BATT_VIN	Not connected to FPGA		
PORT_D[0]	D0	F4	G4/BUS4	48	47	PWM1	H2	D25	PORT_A[3]
PORT_C[5]	A5	B1,D8	G3/BUS3	46	45	GND	Not connected to FPGA		
PORT_C[4]	A4	D1,E8	G2/BUS2	44	43	CAN-TX	J1	D26	PORT_A[4]
PORT_C[3]	A3	E4,E6	G1/BUS1	42	41	CAN-RX	J2	D27	PORT_A[5]
PORT_C[2]	A2	E3,D6	G0/BUS0	40	39	GND	Not connected to FPGA		
PORT_C[1]	A1	E1	A1	38	37	USBH-	K1	D34	PORT_G[0]
Not connected to FPGA			GND	36	35	USBH+	K2	D35	PORT_G[1]
PORT_C[0]	A0	F1	A0	34	33	GND	Not connected to FPGA		
PORT_E[0]	D28	L3	PWM0	32	31	Module Key	Not connected to FPGA		
Not connected to FPGA			Module Key	30	29	Module Key	Not connected to FPGA		
Not connected to FPGA			Module Key	28	27	Module Key	Not connected to FPGA		
Not connected to FPGA			Module Key	26	25	Module Key	Not connected to FPGA		
Not connected to FPGA			Module Key	24	23	SWDIO	M1	D36	PORT_G[2]
PORT_E[1]	D29	M2	TX2	22	21	SWDCK	N2	D37	PORT_G[3]
PORT_E[2]	D30	N3	RX2	20	19	RX1	N6	D38	PORT_G[4]
PORT_E[3]	D31	N7	D1/CAM_TRIG	18	17	TX1	N8	D39	PORT_G[5]
PORT_E[4]	D32	M9	I2C_INT	16	15	CTS1	N9	D40	PORT_G[6]
SCL	SCL	M10	I2C_SCL	14	13	RTS1	N10	D41	PORT_G[7]
SDA	SDA	M11	I2C_SDA	12	11	BOOT (I - Open Drain)	Not connected to FPGA		
PORT_E[5]	D33	M12	D0	10	9	USB_VIN	Not connected to FPGA		
PORT_D[7]	D7	M13	G11	8	7	GND	Not connected to FPGA		
RESET_N	RESET_N	B9	RESET#	6	5	USB_D-	Not connected to FPGA		
Not connected to FPGA			3.3V_EN	4	3	USB_D+	Not connected to FPGA		
Not connected to FPGA			3.3V	2	1	GND	Not connected to FPGA		

Color Key for Board
POWER
SDIO
AUDIO
I2C
UNCAT.
GND
GPIO/BUS
SPIO
DEDICATED
UART

Miscellaneous I/O		
Signal	FPGA Pin	Comments
Clock	H6	Generated on-board
PIN13LED	K10	FPGA output - drives on-board LED
RX	N5	From FTDI driven by USB_D signals
TX	N4	To FTDI driven by USB_D signals
SCL	M10	I2C
SDA	M11	I2C
RESET_N	B9	Reset
TCK	G2	JTAG Connector
TDO	F6	JTAG Connector
TMS	G1	JTAG Connector
TDI	F5	JTAG Connector
JTAGEN	E5	JTAG Connector

Color Key for FPGA		
PORT_C[5:0]	A5-A0	6
PORT_D[7:0]	D07:D00	8
PORT_B[5:0]	D13-D08	6
PORT_A[5:0]	D27-D22	6
PORT_E[5:0]	D33-D28	6
PORT_G[7:0]	D41-D34	8
PORT_H[7:0]	D49-D42	8
Misc		12