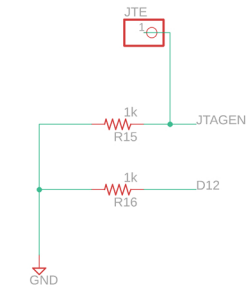
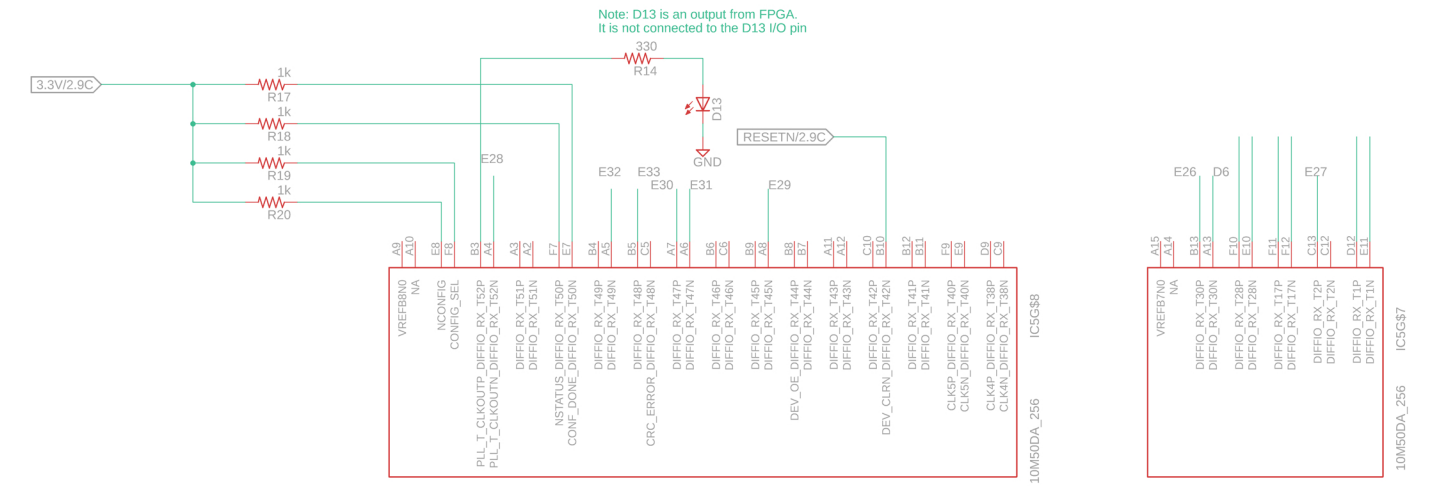


Note: AREF is tied to 3.3v on the back of the board through a cuttable metal track: marked "cut"

Note: Maintenance I2C

Note: External I2C

<h1>Evo M51</h1>	
<h2>Alorium Technology, LLC</h2>	
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SAMD51 <-> M50 <-> board\_edge

FPGA D13/2.9C	EPGA_D13	D13	0132.9C
FPGA D12/2.9C	EPGA_D12	D12	0122.9C
FPGA D11/2.9C	EPGA_D11	D11	0112.9C
FPGA D10/2.9C	EPGA_D10	D10	0102.9C
FPGA D9/2.9C	EPGA_D9	D9	0092.9C
FPGA D8/2.9C	EPGA_D8	D8	0082.9C
FPGA D5/2.9C	EPGA_D5	D5	0052.9C
FPGA D4/2.9C	EPGA_D4	D4	0042.9C
FPGA D1/2.9C	EPGA_D1	D1	012.9C
FPGA D0/2.9C	EPGA_D0	D0	002.9C

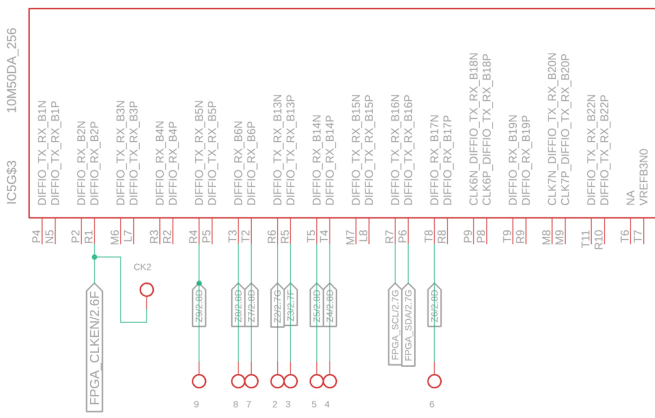
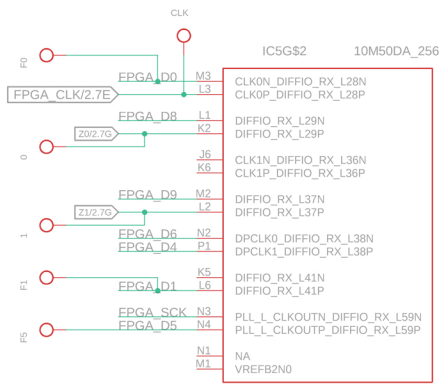
SAMD51 <-> board\_edge

FPGA SCK/2.9C	EPGA_SCK	SCK	0CK2.9C
FPGA MOSI/2.9C	EPGA_MOSI	MOSI	0MOSI2.9C
FPGA MISO/2.9C	EPGA_MISO	MISO	0MISO2.9C

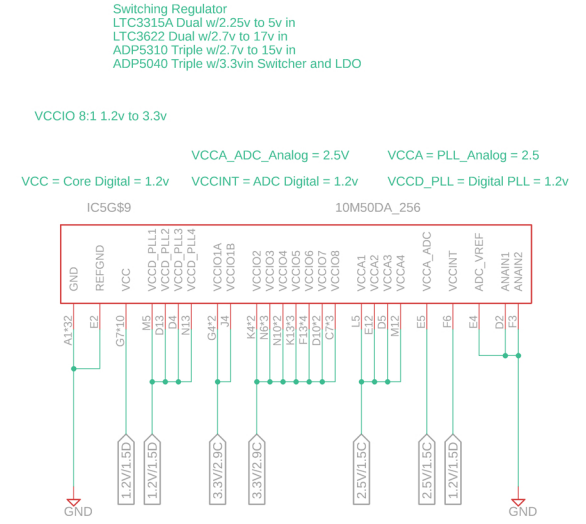
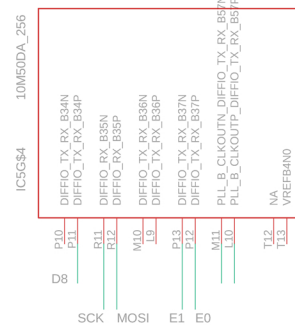
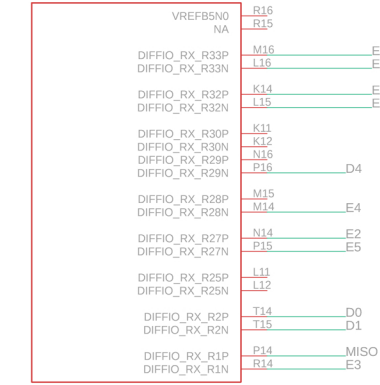
SAMD51 <-> board\_edge

SAMD A0/2.8C	SAMD_A0	A0	0A02.8C
SAMD A1/2.8C	SAMD_A1	A1	0A12.8C
SAMD A2/2.8C	SAMD_A2	A2	0A22.8C
SAMD A3/2.8C	SAMD_A3	A3	0A32.8C
SAMD A4/2.8C	SAMD_A4	A4	0A42.8C
SAMD A5/2.8C	SAMD_A5	A5	0A52.8C

F5	ADC1I1_DIFFIO_RX_L1N
F4	ADC1I2_DIFFIO_RX_L1P
C4	ADC2I1_DIFFIO_RX_L2N
C3	ADC2I8_DIFFIO_RX_L2P
H5	ADC1I3_DIFFIO_RX_L3N
G5	ADC1I4_DIFFIO_RX_L3P
E3	ADC2I3_DIFFIO_RX_L4N
F2	ADC2I4_DIFFIO_RX_L4P
G2	ADC1I5_DIFFIO_RX_L5N
F1	ADC1I6_DIFFIO_RX_L5P
C2	ADC2I5_DIFFIO_RX_L6N
B2	ADC2I6_DIFFIO_RX_L6P
D1	ADC1I7_DIFFIO_RX_L7N
D1	ADC1I8_DIFFIO_RX_L7P
B1	ADC2I7_DIFFIO_RX_L8N
C1	ADC2I2_DIFFIO_RX_L8P
G6	JTAGEN
H2	TMS_DIFFIO_RX_L17N_TMS
H3	TCK_DIFFIO_RX_L17P_TCK
G1	TDI_DIFFIO_RX_L18N_TDI
H1	TDO_DIFFIO_RX_L18P_TDO
J5	DIFFIO_RX_L20N
H6	DIFFIO_RX_L20P
J3	DIFFIO_RX_L22N
J2	DIFFIO_RX_L22P
J1	VREFB1N0



Low Speed = Banks 1A,1B, 8  
High Speed = Banks 2,3,4,5,6,7  
DIFFIO\_TX\_T = True LVDS outputs on TOP side  
DIFFIO\_RX\_L = True LVDS inputs on Left side  
DIFFIO\_RX\_R = True LVDS inputs on Right side  
DIFFIO\_TX\_RX\_B = True LVDS I/O on bottom side  
DIFFIO\_RX\_B = True LVDS inputs on bottom side



## Evo M51

Alorium Technology, LLC

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